1. (Previously presented) An internal stage of a programmable look up table (LUT) circuit for an integrated circuit, comprising:

one or more secondary inputs; and

one or more configurable logic states; and

two or more LUT values; and

a programmable means to select a LUT value from a said secondary input or a said configurable logic states.

2. (Original) The circuit of claim 1, wherein said programmable means is further comprised of selecting a plurality of LUT values, each of said LUT values selected from a secondary input or a configurable logic state.

3. (Original) The circuit of claim 1, further comprising a configuration circuit comprised of one or more user configurable memory elements, wherein:

a memory bit programs said configurable logic state between zero state and one state; and

a memory bit programs said selection between secondary input and configurable logic state.

4. (Original) The circuit of claim 1 further comprising:

a LUT output; and

M primary inputs, where M is an integer value greater than or equal to one, each said M inputs received in true and compliment logic levels; and

2^M LUT values, each said LUT values comprising a configurable logic state or a secondary input, wherein any given combination of said M primary input signal levels couples one

of said LUT values to said LUT output.

5. (Original) The circuit of claim 1, further comprising a thin film transistor.

6. (Previously presented) The circuit of claim 1, wherein said secondary input is comprised one of a logic output, a control signal, a register output and a memory output.

7. (Original) The circuit of claim 1, wherein said programmable method further comprises a means of providing said secondary input as an output when said configurable logic state is selected as a LUT value.

8. (Previously presented) The circuit of claim 1, wherein a secondary input is an output of a K-LUT circuit, said K-LUT circuit comprising:

a LUT output; and

K inputs, wherein K is an integer value greater than or equal to one, each said K inputs received in true and compliment logic levels; and

2^K LUT values, each said LUT values comprising two configurable logic states.

9. (Original) The circuit of claim 2, wherein said memory element is selected from one of fuse links, anti-fuse capacitors, SRAM cells, DRAM cells, metal optional links, EPROM cells, EEPROM cells, flash cells, ferro-electric elements, optical elements, electro-chemical elements and magnetic elements.

10. (Currently amended) A sub-circuit of a programmable look up table macro circuit for an integrated circuit, comprising:

M primary inputs, wherein M is an integer value greater than or equal to one, and each said M inputs received in true and compliment logic levels; and

2^M secondary inputs; and

2^M configurable logic states, each said state comprising a logic zero and a logic one; and

2^M LUT values; and

a programmable means to select each of said LUT values from a said secondary input or a said configurable logic state.

11. (Original) The circuit of claim 10, further comprising a configuration circuit comprised of a plurality of user configurable memory elements, wherein:

a memory bit programs each of said configurable logic states between zero state and one state; and

a memory bit programs each of said LUT value selections between a secondary input and a configurable logic state.

12. (Original) The circuit of claim 10, wherein each of said secondary inputs is further comprised of an output of a previous K-LUT circuit, said K-LUT circuit comprising:

a LUT output; and

K inputs, wherein K is an integer value greater than or equal to one, and each said K inputs received in true and compliment logic levels; and

2^K LUT values, each said LUT values comprising two configurable logic states.

13. (Original) The circuit of claim 10, further comprising a thin film transistor.

14. (Original) The circuit of claim 11, wherein said memory element is selected from one of fuse links, anti-fuse capacitors, SRAM cells, DRAM cells, metal optional links, EPROM cells, EEPROM cells, flash cells, ferro-electric elements, optical elements, electro-chemical elements and magnetic elements.

15. (Original) The circuit of claim 12, wherein programmable selection of one or more of said secondary inputs as LUT values further comprises implementing a (K+M) input LUT function.

16. (Original) The circuit of claim 12, wherein programmable selection of 2^M configurable logic states as LUT values further comprises implementing a M-LUT function decoupled from 2^M other K-LUT functions.

17. (Original) A programmable macro look up table (macro-LUT) circuit for an integrated circuit, comprising:

a plurality of LUT circuits, each of said LUT circuits comprising a LUT output, at least one LUT input, and at least two LUT values; and

a programmable means of selecting LUT inputs to at least one of said LUT circuits from one or more other LUT circuit outputs and external inputs, and selecting LUT values to at least one of said LUT circuits from one or more other LUT circuit outputs and configurable

logic states, said programmable means further comprised of two selectable manufacturing configurations, wherein:

in a first selectable configuration, a random access memory circuit (RAM) is formed, said memory circuit further comprising configurable thin-film memory elements;

in a second selectable configuration, a hard-wire read only memory circuit (ROM) is formed in lieu of said RAM, said ROM duplicating one RAM pattern in the first selectable option.

18. (Original) The circuit of claim 17, further comprising one or more registers to latch data from one or more of said LUT outputs.

19. (Original) The circuit of claim 17, wherein said RAM element is selected from one of fuse links, anti-fuse capacitors, SRAM cells, DRAM cells, metal optional links, EPROM cells, EEPROM cells, flash cells, ferro-electric elements, optical elements, electro-chemical elements and magnetic elements.

20. (Original) The circuit of claim 17, further comprising a macro LUT response time characteristic, said response time comprising a transit time of a LUT value to a macro LUT output, wherein said response time is substantially identical between the two selectable manufacturing configurations.